Area and power optimized implementation of MT-CMOS of 8x8 Multiplier using
Urdhva Tiryakbhayam Algorithm

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Abstract: Now a days in the market everyone is having interest in choosing the product which consume less power. In which it plays an imperative role specifically in the field of VLSI today, every designer be it an analog circuit or a digital circuit designer is concerned about the amount of power his or her circuit is going to consume in the end. The overview of the paper is in which they undergo the multiplication process of ancient scientist named as Vedas by this approach here it comes, introduction of a novel and high performance design of an 8x8 multiplier using Urdhva Tiryakbhayam Algorithm. We have presented three different designs of the 8x8 Vedic multiplier using the CMOS technology, PTL and finally concoct the Vedic Multiplier using the Multi-Threshold Voltage CMOS (MTCMOS) and proved that the MTCMOS implementation of Vedic Multiplier is the best among all the implementations. The multiplication process is carried out from ancient technology. The functionality of all the three designs and there PDP and total power consumptions and three different voltages were calculated on tanner EDA. The proposed MTCMOS implementation of Vedic multiplier is up to 24.55% power efficient and about 97.54% speedy as compared to the conventional CMOS implementation of Vedic multiplier.

I. INTRODUCTION

Vedic Mathematics is one of the most ancient methodologies used by the Aryans in order to perform mathematical calculations. This consists of algorithms that can boil down large arithmetic operations to simple mind calculations. The above said advantage stems from the fact that Vedic mathematics approach is totally different and considered very close to the way a human mind works. The efforts put by Jagadguru Swami Sri Bharati Krishna Tirtha Maharaja to introduce Vedic Mathematics to the commoners as well as streamline Vedic Algorithms into 16 categories or Sutras needs to be acknowledged and appreciated. The Urdhva Tiryakbhayam is one such multiplication algorithm which is well known for its efficiency in reducing the calculations involved. With the advancement in the VLSI technology, there is an ever increasing quench for portable and embedded Digital Signal Processing (DSP) systems. DSP is omnipresent in almost every engineering discipline. Faster additions and multiplications are the order of the day. Multiplication is the most basic and frequently used operations in a CPU. Multiplication is an operation of scaling one number by another. Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Transforms, etc. With ever increasing need for faster clock frequency it becomes imperative to have faster arithmetic unit. Therefore, DSP engineers are constantly. The word “Vedic” was coined from the word “Veda” which means the repertoire of all knowledge. Vedic mathematics is commonly based on 16 Sutras (or aphorisms) dealing with different types of mathematics like arithmetic, algebra, geometry etc. The essence of Vedic mathematics is the fact that it reduces the otherwise ponderous calculations in conventional mathematics that slows down the calculation process considerably. This is because the Vedic formulas are predicated on the principles which are generally used by humans. This is a very enticing field and presents some efficient algorithms which can be applied to numerous branches of engineering such as computing, image processing and digital signal processing. This paper deals with various multipliers implemented using CMOS logic style and their comparative analysis on the basis of power and PDP (Power delay product). A variety of multipliers have been reported in the literature [6]-[8] but power dissipation and area used by these multiplier circuits are relatively large. This paper proposed a high performance and power efficient 8x8 multiplier design based on Vedic mathematics using CMOS logic style. This paper is structured as follows. Section II surveys the basic fundamentals of Vedic multiplication techniques. Section III describes array multiplier and proposed multiplier design. Section V deals comprises the introduction of MTCMOS technique. Comparative analysis of both the multipliers on the basis of power and PDP is done in Section VI. Finally Section VII comprises of Conclusion. References are given at the end of paper.
II. VEDIC MULTIPLICATION METHOD

Vedic mathematics is a mathematical system consisting of sixteen basic Sutras (i.e. formulas) given by Shri Bharati Krishna Tirhaji Maharaja during the 20th century. All sixteen sutras have their own individual significance. The Urdhva-Tiryagbyham means vertically and crosswise, Ekadhikina Purvena means next is one more than previous, Nikhilam Navatashcaramam Dashatah means all are subtracted from 9 and the last is subtracted from 10, Paraavartya Yojayet means transpose and then adjust, Shunyam Saamyasamuccaye means when the sum is same then that sum is zero, (anurupy) Shunyamanyat means if one is in ratio then other is zero, Puranapuranabhyham means completion and non-completion, Chalana-Kalanabhyham means differences and similarities, Yaavadunam means whatever the amount of its deficiency, Vyasytisanamstih means part and whole, Shesanyankena Charamena means last digit’s remainder, Sopaantyadvayamantyam means the ultimate and twice of the penultimate, Ekanyunena Purvena means by one less than previous one, Gunitasamuchyah means the sum’s product is equal to the product’s sum, Gunakasamuchyah means the sum’s factor is equal to the factor’s sum.

These Sutras have been majorly used for the multiplication of two numbers in the decimal format. In this work, we extrapolated the same ideas to the binary number to make the proposed algorithm compatible with the digital hardware. From the above defined sixteen sutras we are using one sutra that is Urdhva-Tiryagbyham to implement the Vedic multiplier

A. Urdhav-Tiryagbyham rule

It is the general sutra that is the formula perfectly for all types multiplication. It means “vertically and crosswise” as shown

**URDHAV RULE**

Urdhva Tiryakbhayam (UT) is a multiplier based on Vedic mathematical algorithms devised by ancient Indian Vedic mathematicians. Urdhva Tiryakbhayam sutra can be applied to all cases of multiplications viz. Binary, Hex and also Decimals. It is based on the concept that generation of all partial products can be done and then concurrent addition of these partial products is performed. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhayam. Unlike other multipliers with the increase in the number of bits of multiplicand and/or multiplier the time delay in computation of the product does not increase proportionately. Because of this fact the time of computation is independent of clock frequency of the processor. Hence one can limit the clock frequency to a lower value. Also, since processors using lower clock frequency dissipate lower energy, it is economical in terms of power factor to use low frequency processors employing fast algorithms like the above mentioned. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases at a slow pace as compared to other conventional multipliers. To understand the concept of Urdhav rule algorithm, let us consider the example of multiplication of two numbers N1=41 and N2=32. The process is followed according to the steps shown in Fig. 2.

Firstly, we need to multiply the unit digit of the two numbers vertically that is multiplication of 1 and 2. Step 2 consists of crosswise multiplication of unit digit to tens digit of first number and unit digit of first to tens digit of second number and then addition of the results of two crosswise multiplications is done, that is addition of 8(product of 4 and 2) and 3(product of 1 and 3) giving carry as 1. In step 3 vertical multiplication of the digits at tens place is carried out giving 12 (multiplication of 4 and 3). In step 4 the result of step 3 is added with the carry generated in the step 2 giving 13(addition of 12 and 1). The result is produced by writing the result of step 4, the digit obtained by eliminating the carry in the result of step 2 and the result of step 1 as 1312.

![Fig. 2. Multiplication example of two numbers.](image-url)
III. HYBRID PRL/CMOS

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input. If several devices are chained in series in a logic path, a conventionally constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Since there is less isolation between input signals and outputs, designers must take care to assess the effects of unintentional paths within the circuit. For proper operation, design rules restrict the arrangement of circuits, so that sneak paths, charge sharing, and slow switching can be avoided. Simulation of circuits may be required to ensure adequate performance. Pass transistor is the logic design in which the primary inputs drive the gate terminals and source-drain terminals in contrast to static CMOS where primary inputs drive gate terminals. Source side of logic transistor networks is connected to some input signals instead of the power lines. One of the main advantages of this logic style is that only one pass transistor network (either NMOS or PMOS) is sufficient to perform the logic function thereby using ptl one can save on the hardware requirements for the implementation of any circuit. Inverters are usually attached to the gate output to provide acceptable output driving capabilities. To understand the functioning of ptl design we will consider the implementation of a two input XNOR gate (fig.3) which uses only two nmos transistors. XNOR gate outputs logic high (1) when the two inputs are same that is logic-1 for inputs 00 and 11 and logic low (0) otherwise. Now when A = 1 then the lower nmos will function and the upper nmos will be in off mode and so the input connected to lower nmos that is B will transfer to the output out. When A= 0 then the upper nmos is in function and lower nmos will be in off mode and so the input connected to the upper nmos will transfer to the output.

XNOR using Transmission gate

To give an explicit picture of how ptl reduces the number of transistors used in any circuit we can compare the above stated ptl implementation of xnor with cmos implementation of xnor.

XNOR using CMOS

Cmos implementation of xnor uses 8 transistors adding to the power consumer of the circuit considerably whereas the same function can be implemented using only two transistors by ptl logic. Hence using ptl logic we can not only reduce the hardware requirements for the circuit by reducing the number of transistors required which intern helps in reducing the power consumption of the circuit. Though ptl logic style reduces the number of transistors used for the implementation of any logic function it does not give full swing as in the case of cmos , every ptl logic design must realize a multiplexer structure in addition to these two drawbacks layout designing of ptl logic style is not
straight forward and efficient. To overcome these pitfalls in the ptl logic style instead of using purely ptl logic style we use hybrid ptl/cmos logic which incorporates the advantages of both ptl and cmos.

IV. MULTIPLIER
A. Vedic Multiplier
The hardware implementations of 2x2, 4x4 and 8x8 Vedic Multiplier are carried out using “Urdhava-Triyakbhyam”(Vertically and Crosswise) sutra for multiplying two binary numbers. Here, both Partial product generation and addition is performed concurrently. Therefore, it is adaptive to parallel processing.

Block diagram of 2x2 bit Vedic multiplier.
The implementation of 2x2-bit Vedic multiplier is structured by using four AND gates and two HA as shown in Fig. 5. The 1st HA is used to add outputs of AND gates having input a1b0 & a0b1 and 2nd HA are used to add carry generated from 1st HA and output of AND gate having input a1b1. Similarly, Consider an example of a 4x4-bit Vedic multiplier unit as shown in Fig. 6 which multiplies two 4-bit numbers (A and B), each number can be expressed as (A0–A3, B0– B3); A3 and B3 being the most significant

4x4 bit Vedic multiplication method.
Each square shape block in the above figure shows a 2x2 bit Vedic multiplier unit. First 2x2 bit Vedic multiplier has inputs as A1A0 and B1B0. The last block is also 2x2 bit Vedic multiplier with inputs A3 A2 and B3 B2. The blocks in the middle are 2x2 bit multipliers with inputs A3 A2 & B1B0 and A1A0 & B3 B2. So the final result of multiplication will be of 8 bit as S7S6S5S4S3S2S1S0. To understand the concept, the Block diagram of 4x4 bit Vedic multiplier is to get final product (s7 s6 s5 s4 s3 s2 s1 s0), four 2x2 bit Vedic multipliers and three 4-bit Ripple-Carry (RC) Adders are required.
Thus, we can implement NxN bit Vedic multiplier for N bits. Hence, we can improve efficiency and performance.

V. VEDIC MULTIPLIER USING MTCMOS TECHNIQUE

The new MTCMOS circuit technology is proposed to satisfy both requirements of lowering the threshold voltage of a MOSFET and reducing stand-by current, both of which are necessary to obtain high-speed low-power performance at a This technology has two main features. One is that Nchannel and P-channel MOSFET’s with two different threshold voltages are employed in a single chip. The other one is two operational modes, “active” and “sleep,” for efficient power management. shows the basic MTCMOS circuit scheme with the NAND gates. The logic gate is composed of MOSFET’s with a low threshold voltage of about 0.2-0.3 V. Its power terminals are not connected directly to the power supply lines VDD and GND, but rather to the “virtual” power supply lines VDDV and GNDV. The real and virtual power lines are linked by MOSFET’s Q1 and Q2. These have a high threshold voltage of about 0.5-0.6 V and serve as sleep control transistors. Signals SL and E, which are connected to the gates of Q1 and Q2, respectively, are used for activelsleep mode control. Circuit operation in each mode at a supply voltage of 1 V is described below. Vdd of 1 v .Additionally, it is the leakage current which is the prime source of energy consumption in an idle circuit. In various hand-held battery-operated gadgets like mobile phones, laptops etc. employs long standby periods thus reducing the leakage current is highly important to provide longevity to the battery. The highly recommended circuit technique for the leakage current reduction is the Multi-Threshold Voltage CMOS (MTCMOS). In MTCMOS technology, efficient power management is obtained by allowing the circuit to operate in two modes: 1) Active Mode 2) Sleep Mode. The conventional circuit works using a single threshold voltage (Vt) whereas the circuits employing the MTCMOS technique works on two different threshold voltage switches i.e. the Low Vt and High Vt . The circuit makes use of two different set of transistors – one being the High Vt transistors known as the “sleep” transistors and other being the Low Vt transistors which forms the logical circuit. The sleep transistors helps in the reduction of leakage current thus providing the high performance and the Low Vt transistors are used to boost the circuit’s speed performance.

Power Gating Techniques using MTCMOS

The power gating technique used in MTCMOS. The above circuit comprises of two sleep transistors S1 and S2 which possess the higher Vt . The logical circuit between S1 and S2 comprises of the Low Vt transistors is not connected directly to the real supply, Vdd and ground, Gnd but is connected to virtual supply and ground lines Vddv and Gndv. The sleep transistors are provided with complementary inputs S and SBAR. The circuit works in the active mode when, S=0 and SBAR=1 thus making both the sleep transistors S1 and S2 to remain ON and the virtual supply and ground lines Vddv and Gndv works as real supply lines and the logic circuit performs its operations normally at higher speed. But when S=1 and SBAR=0, the circuit works in the sleep mode making S1 and S2 sleep transistors to go in OFF state which results in the floating of virtual power supply lines and sleep transistors S1 and S2 suppresses the large leakage current present in the circuit. This reduces the power consumption as the leakage current has been lowered.
XNOR using MTCMOS Technique. The above Fig.10 represents the implementation of XNOR using the MTCMOS technique. Here a high Vt transistor i.e. the sleep nMOS transistor is incorporated at the bottom of the logical circuit design which during the sleep mode helps in the abatement of the leakage current present in the circuit thus reducing the overall power consumption.

VI. COMPARISON AND RESULTS

Implementation of 8x8 bit Vedic multiplier using CMOS logic, PTL logic and using MTCMOS technique using the 50nm technology has been carried out on Tanner EDA tool. Power consumption and Power Delay Product (PDP) comparsons for 8x8 bit Vedic-CMOS, 8x8 bit Vedic-PTL and 8x8 bit MT-Vedic multipliers at different voltages and for 50MHz and 100 MHz frequencies is shown in Table 1. The comparison tables shows Power comparison and PDP for all the three types of Vedic 8x8 bit multipliers for 1v, 2v and 3v. Tables explicitly show that PTL implementation of Vedic multiplier has less power consumption as compared to 8x8 Vedic multiplier implemented using CMOS. At 1v for 50MHz there is a reduction of 11.37% in power consumption by Vedic-PTL as compared to Vedic-CMOS. But at same set of values MTVedic outperforms Vedic-PTL by providing a 14.86% power reduction. Similarly comparing there PDP’s at 2v for 50MHz Vedic-PTL has 91.48% reduced PDP than Vedic-CMOS and MT-Vedic again outperforms Vedic-PTL by showing a 71.13% reduced PDP. The conclusion that we can draw from this is that MT-Vedic outshines both Vedic-PTL and CMOS in power consumption and PDP and shows 24.55% in power consumption and 97.54% reduction in PDP compared to Vedic-CMOS.

VII. CONCLUSION

In VLSI Design the mean intension is to reduce the size of chip ,by using different techniques and Here in VEDIC Multiplier we cross check of area, delay, Power & Accuracy which give greater advantage .The MTCMOS implementation of vedic multiplier which give high performance compare to the previous multipliers in terms of Power in which it acquired 24% and in terms of speed also it very highly executed when compare to conventional multipliers .

REFERENCES


