DESIGN OF 16-BIT SUCCESSIVE APPROXIMATION ANALOG TO DIGITAL CONVERTER IN 180nm CMOS TECHNOLOGY

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ABSTRACT

Nowadays, a larger percentage of mixed-signal applications require energy limited system solutions. Analog to Digital Converters (ADCs) are critical component in most of such systems, hence the stringent requirements on energy consumption requests the ADC design to be low power. Among various ADC architectures, we chose to implement a Successive Approximation Register (SAR) ADC that is one of the best suited for low power.

Successive Approximation Register (SAR) analog-to-digital converters (ADCs) achieve very low power consumption due to its simple architecture based on dominant digital content. Main limitation of SAR ADCs is low sample rate, which linked to its serial decision making nature.

This work proposes an approach for designing a 16 bit successive approximation analog to digital Converter which could be made to operate at low voltage supply by efficiently exploiting the comparator architecture and analyzes the effect of various parameters on the characteristics, which operates at 2.5V power supply in 180nm CMOS technology. In amplifier trade-off curves are computed between all characteristics such as gain and phase margin. The comparator is designed in 180nm technology and exhibits a gain of 53.6dB with a phase margin of 179 degrees where the operating point is 1.49v. Sample and Hold circuit is designed in 180nm technology Designed architecture of R/2R DAC operates at a 2.5V power supply and simulation results are verified using virtuoso and are presented.

I. INTRODUCTION

Comparing Successive Approximation Register, Flash, Folding and Interpolating and Sigma-Delta ADCs, the SAR ADC seems allowing the lowest-power consumption. This architecture has the advantage to be very simple; it implements the binary search algorithm.

Power dissipation scales with the sample rate, unlike flash ADCs that usually have constant power dissipation versus sample rate. This is especially useful in low-power applications. Moreover SAR ADC does not contain an operational amplifier; that are generally power-hungry, it needs just one comparator that consume much less power than operational amplifiers.

SAR ADC has four mains building blocks they are Sample and Hold Stage (S/H), Digital to Analog Converter (DAC), Comparator and Successive Approximation Register (SAR)

The algorithm is very similar to like searching a number from telephone book. For example, to search a telephone number from telephone book, first, the book is opened and the number maybe located either in first half or in the second half of the book. Further, relevant section is divided into half. This procedure can be followed until finding relevant number.

Figure1.1 SAR ADC block diagram

II. IMPLEMENTATION

Comparator Differential Gain Stage:

Transistors M1, M2, M3, and M4 form the first stage of the op amp the differential amplifier. Transistors M1 and M2 are N channel MOSFET (NMOS) transistors which form the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage.

Second Gain Stage:

Consisting of transistors M6 and M7, this stage takes the output from the drain of M2 and amplifies it through M6. Again, similar to the differential gain stage, this stage employs an active device, M7, to serve as the load resistance for M6. The gain of
this stage is the transconductance of M6 times the effective load resistance comprised of the output resistances of M6 and M7. M7 is the driver while M5 acts as the load.

Bias String:
The biasing of the operational amplifier is achieved with only four transistors. Transistors M8 form a simple current mirror bias string that supplies a voltage between the gate and source of M5. Transistors M7 and M8 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string. M8 connected to ensure they operate in the saturation region.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1=M2</td>
<td>W=0.54u,L=0.18u</td>
</tr>
<tr>
<td>M3=M4</td>
<td>W=2.7u,L=0.18u</td>
</tr>
<tr>
<td>M5=M8</td>
<td>W=0.81u,L=0.18u</td>
</tr>
<tr>
<td>M6</td>
<td>W=16.92u,L=0.18u</td>
</tr>
<tr>
<td>M7</td>
<td>W=2.52u,L=0.18u</td>
</tr>
<tr>
<td>IBIAS</td>
<td>30uA</td>
</tr>
<tr>
<td>Cc,CL</td>
<td>3pF,10pF</td>
</tr>
<tr>
<td>VDD</td>
<td>2.5v</td>
</tr>
</tbody>
</table>

Table1. Design parameters of two stage op-amp

R/2R DIGITAL TO ANALOG CONVERTER
The R/2R network is build by a set of resistors of two values, with values of one sets being twice of the other. In all of the circuits sets of 1K and 2K resistors are used, which is near to the R/2R ratio. Accuracy or precision of DAC depends on the values of resistors chosen, higher precision can be obtained with an exact match of the R/2R ratio.

The inputs to the ladder are fed from an N-bit input. The input voltages range from 0V to 2V. Here R-2R network is also converted in to the CMOS equivalent circuits. This configuration consists of a network of resistors alternating in value of Rand 2R. Starting at the right end of the network, notice that the resistance looking to the right of any node to ground is 2R. Each node voltage is related to Vref, by a binary-weighted relationship caused by the voltage division of the ladder network. The total current flowing from Vref is constant. The output voltage, Vout is determined.

Sample and Hold
A sample and hold (S/H) or track-and-hold (T/H) circuit is frequently required to capture rapidly varying signals for subsequent processing by slower circuitry. In track mode, the T/H functions as a simple buffer amplifier. While in the hold mode two effects are of primary importance. The first is droop which describes the decay of the output signal as energy is lost from the storage element (usually a capacitor) within the T/H circuit.

In the circuit when S1 turns on and injects charge onto holding capacitor C_H, when S1 turns off and discharges charge onto holding capacitor C_H, then complete cancellation occurs and the held voltage on C_H is not corrupted by charge injection.
Successive approximation register

Successive Approximation Register (SAR) control logic determines each bit successively. The SA register contains N bit for an N-bit ADC. There are 3 possibilities for each bit, it can be set to ‘1’, reset to ‘0’ or keeps its value. In the first step, MSB is set to ‘1’ and other bits are reset to ‘0’, the digital word is converted to the analog value through DAC. The analog signal at the output of the DAC is inserted to the input of the comparator and is compared to the sampled input. Based on the comparator result, the SAR controller defines the MSB value. If the input is higher than the output of the DAC, the MSB remains at ‘1’, otherwise it is reset to ‘0’. The rest of bits are determined in the same manner. In the last cycle, the converted digital word is stored. Therefore, an N-bit SAR ADC takes N+1 clock cycles to perform a conversion. Successive approximation register ADC implements the binary search algorithm using SAR control logic. In general, there are mainly two fundamentally different approaches to designing the SAR logic.

III. SIMULATION RESULTS

To analyze the behavior of SARADC, first discuss the results of basic design of comparator. Comparator operates at 2.5V power supply in 180nm CMOS technology. Here results are computed between characteristics such as gain, phase margin of op-amp which is used as comparator and 16bit DAC, sample and hold circuit and SAR logic. The comparator is designed in 180nm technology and obtained a gain of 53.6db with a phase margin of 179 degrees in ac analysis with a start frequency from 100Hz and stop frequency of 1000 MHz where the operating point is 1.49V resulted from dc analysis.

Figure 1.7 Comparator Transient Response

Above figure 1.10 Comparator operates at 2.5V power supply in 180nm CMOS technology. The comparator transient response is computed by giving a input voltage of 1.5V.

Figure 1.8 Comparator DC Response

Above figure 1.11 Comparator operates at 2.5V power supply in 180nm CMOS technology. Here DC analysis is computed where it's operating point is1.49V. Here all the transistors are set to be operated in saturation region. Its start and stop response is given from 0 to 2.5

Figure 1.9 Comparator AC Response
Above figure 1.12 Comparator operates at 2.5V power supply in 180nm CMOS technology. Here AC analysis is computed where it’s gain and phase margin are resulted. Gain of 53.6db with a phase margin of 179 degrees in ac analysis is obtained with a start frequency from 100Hz and stop frequency of 1000 MHz.

Figure 1.10 16 bit R/2R DAC Transient Response.

Above figure 1.13 16 bit R-2R bit Digital to Analog Converter (DAC) which could be made to operate at low voltage supply of 2.5V by efficiently exploiting the two stage Operational Amplifier (Op-Amp) architecture in 180nm CMOS technology. Output errors due to resistor tolerances are often overlooked in the design of the digital to analog conversion (DAC) circuit and in the selection of the R/2R ladder itself. Here the inputs are given of different clock pulses as mentioned in the above table4

Figure 1.11 Sample And Hold Output

Above figure 1.14 the input voltage is given with amplitude of 5mv and the holding capacitor is 5pf. The frequency is said to be of 10 kHz. Time period is 10us and pulse width is given as 5us.

SAR logic is usually a decision register and decision logic. Serial in serial out shift register is designed in 180nm technology. SISO is designed by using d flip-flop. Time period is 10us and its pulse width is given as 5us. Input is given as 1V.

16 bit SAR ADC is designed using 180nm technology containing the blocks comparator,R-2R DAC,sample and hold circuit and SAR logic: all the blocks are designed using 180nm technology. The gain of the comparator is 53db and the phase margin is 173 degrees. The input is given to the sample and hold, the input is 0.6V with an amplitude of 5mv. frequency is said to be 1.25MHZ. The holding capacitor is 5PF. The clock is given to the shift register with a period of 10us and pulselength of 5us. Reference voltage (vref) is given to DAC which is of 1.25V. The SAR ADC is operated at a power supply of 2.5V.

Figure 1.12 SAR logic output

IV. CONCLUSION

This thesis presents implementation of a 16-bit SAR ADC operating at 1.25 MHz and supply voltage of 2.5 V in 180nm CMOS technology. The ADC employs an R-2R DAC, a comparator, sample and hold and a SAR control logic containing a shift register.

With an increasing trend to a system-on-chip, DAC has to be implemented in a low-voltage submicron CMOS technology in order to achieve low manufacturing cost while being able to integrate with other circuits. Experiments were performed on 16 bit R2R DAC. From this results could conclude that conversion is performed for all combination successfully and a low-power 16-bit R-2R DAC in an 180nm CMOS technology with a 2.5V supply voltage is designed.
Designing the comparator is a crucial part of ADC design. In this work, comparator performance metrics are studied, such as gain, phase margin in ac analysis and operating point of 1.49V dc analysis. Based on these studies, comparators are implemented and compared regarding power consumption, speed, and accuracy. Consequently, the comparator is selected to be used in the designed ADC.

The main advantage of SAR ADC is good ratio of speed to power. The SAR ADC has compact design compare to flash ADC, which makes SAR ADC inexpensive. The physical limitation of SAR ADC is, it has one comparator throughout the entire conversation process. If there is any offset error in the comparator, it will reflect on the all conversion bits. The other source is gain error in DAC. However, the static parameter errors do not affect dynamic behaviour of SAR ADC. Furthermore, higher the speed, it is difficult to obtain the dynamic behaviour of ADC.

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